Serial No. 10/056,610
Docket No. – MIO 0051 V2

## Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Please amend claim 40 as follows:

1-29. (Canceled)

30. (Previously Amended) A method of encapsulating an integrated circuit comprising:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer into said underlying substrate, but not as far as said second major face; and

encapsulating said semiconductor chip and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

31. (Canceled)

32. (Previously Amended) A method of forming a laminate to lock an encapsulant comprising:

forming at least one continuous laminate layer;

forming a second laminate layer over said continuous laminate layer, so as to define an underlying cavity;

forming a third laminate layer over said second laminate layer, so as to define a void portion over said underlying cavity;

forming a fourth laminate layer over said third laminate layer, so as to define a void portion over said void portion of said third laminate layer;

forming a conductive layer over said fourth laminate layer, so as to define a void portion over said void portion of said fourth laminate layer; and

forming a solder resist layer over said conductive layer, so as to define a void portion over said void portion of said conductive layer.

33. (Previously Amended) The method of claim 32, wherein said underlying cavity, said void portion of said third laminate layer, said void portion of said fourth laminate layer, said void portion of said conductive layer and said void portion of said solder resist layer are formed to collectively form a void.

34. (Previously Amended) The method of claim 33 further comprising:

placing a die over at least a portion of said solder resist layer; and

forming an encapsulant over said solder resist layer, over said die and in said void.

35–39. (Canceled)

40. (Currently Amended) A method of encapsulating an integrated circuit comprising:

providing a die;

providing a substrate having at least one continuous laminate layer and at least one resin layer over said continuous laminate layer;

forming at least one laminate layer over said at least one resin layer;

forming a void in said at least one resin layer and said at least one laminate layer such that a portion of said void located in said at least one resin layer is below a remaining portion of said at least one laminate layer, wherein said void does not extend through said continuous laminate layer such that said continuous laminate layer is a bottom to said void;

placing said die over said at least one laminate layer; and

encapsulating said die by forming encapsulant over said at least one laminate layer, over said die and in said void.

41. (Previously Amended) The method of claim 40, wherein said at least one laminate layer is formed by forming a conductive layer over said at least one resin layer and forming a solder resist layer over said conductive layer.

42. (Previously Amended) The method of claim 40, wherein said void is formed by forming an underlying cavity in said at least one laminate layer.

43. (Previously Amended) The method of claim 40, wherein said encapsulant is formed in substantially all of said void.

44. (Previously Amended) The method of claim 40, wherein said at least one resin layer is formed from bismaleimide triazine laminate.

45. (Previously Amended) The method of claim 40, wherein said at least one resin layer is formed from FR-4 epoxy-glass laminate.

46-49. (Canceled)

50. (Previously Amended) The method of claim 33, wherein said void has a varying profile.

51. (Previously Amended) The method of claim 50, wherein said void having a varying profile is formed by a process selected from the group consisting of drilling, stamping, chemical etching, and combinations thereof.

52. (Previously Amended) The method of claim 50, wherein said void having a varying profile is formed having a T-shaped profile.

53. (Previously Presented) The method of claim 33, wherein said void extends into said laminate, but not entirely through said continuous laminate layer.